Cost-Competitive, High-Performance, Highly Reliable Power Devices on Si licon Carbide and Gallium Nitride

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04/29/2022

2022 DOE Annual Merit Review

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Project ID # elt247

Overview

Timeline

- Project start April 2019
- Project end March 2024
- Percent Complete: 60%

Budget

- BP3 total $333K: Federal $ 30 0K+ cost share (10%)

Barriers

- Cost: the lack of device innovations and processing technologies
- Performance: need state-of-the-art facility for tight design rules
- Reliability and ruggedness: trade off relationship with performance

Partners

- Sandia National Laboratories
- The Ohio State University
- SiCamore

Relevance – objectives / impact

Overall objectives in this project

- The primary objective of this project is to ensure that the next-generation of wide-bandgap devices of sufficient performance, reliability, and price to achieve the system-level DOE goals.

Objectives in previous period (BP3, FY2021-2022)

- Establishment of the process baseline for Gen3 MOSFETs.
- Evaluation of Gen3 MOSFETs;

  Performance; Ron,sp=4mohm-cm^2, Vth=2V, BV=1700V.

  Reliability; TDDB 10 C/cm^2,PBTI<0.5V, HTRB 1000hrs at 1460V.

  Ruggedness; Short Circuit SOA 4µs.

Impact of research

- The successful development of the proposed device will bring in a highly efficient and reliable power electronics for electric drive trains.

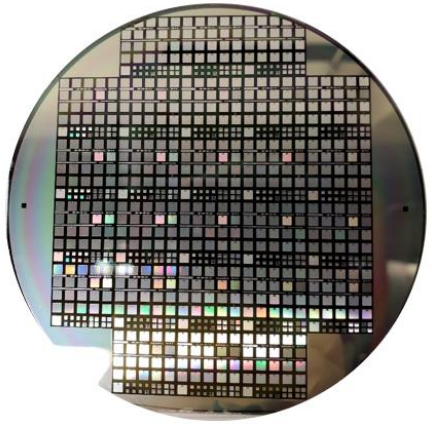
Milestones – BP4

Milestone	Type	Description
Gen4 SiC MOSFET Design	Technical	The cell and edge termination structures for MOSFETs and JBS diode integrated MOSFETs have been optimized; Optimized devices included in a single mask-set.
Gen4 SiC MOSFETs Fabrication	Technical	Two qualification lots to make Gen4 devices completed.
Gen4 SiC MOSFETs Evaluation	Technical	Static performances have been characterized on-wafer; Reliabilities and ruggedness evaluated.
AlGaN/GaN HEMT devices on sapphire and HVPE GaN	Technical	Static Performance characteristics have been made on-wafer and on-processed devices.
Improved static performance, Reliability assessment on Gen4 devices	Go/No Go	Performances of Gen4 SiC MOSFETs evaluated: BV = 1700V, $R_{on,sp}$ = 4 mohm-cm^2, V_{th} = 2V Short Circuit SOA 6µs; Avalanche energy 8 J/cm^2; TDDB 12 C/cm^2; PBTI < 0.3V (at Vgs=20V); NBTI <-0.5V (at Vgs=-5V); HTRB 1000hrs at 1540V; dv/dt 500kV/µs; 3Q diode behavior +-10% change.

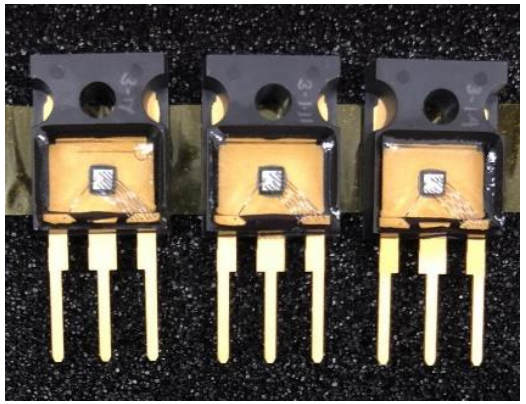
Approach – CPR metrics

	on-resistance	chip price	blocking behavior	threshold voltage	short circuit capability	avalanche capability	HTRB	HTGB, Vth stability	dv/dt, switching behavior	BPD, SF- degradation	thermal management	others
short channel	+	+	-	-	-		-	-				
tight cell pitch	+	+			-							
self aligned channel	+	+	+	+				+				
narrow JFET region			+		+	+	+		+			
enhanced doping in JFET	+				-	-	-					
deep Pwell (so is JFET region)			+		+	+	+					
thinner gate oxide	+			-	-		-	-				
innovative gate oxide process	+	+		+	+			?		+		
unipolar diode integration		+							+	+		
inversion mode channel	-	-	+	+	+			+				
source doping reduction	-				+							
reduction in Wp+/Wn+	+	+			-	-						
Ringe based edge termination		-	-			-	-		+			
JTE based edge termination		+	+			+	+		-			
substrate thinning	+										+	
double sided package									+		+	
Ion implants @ RT		+								?		
W plug(high aspect ratio CT)	+										+	+
Striped cell design	-		+		+		+				+	

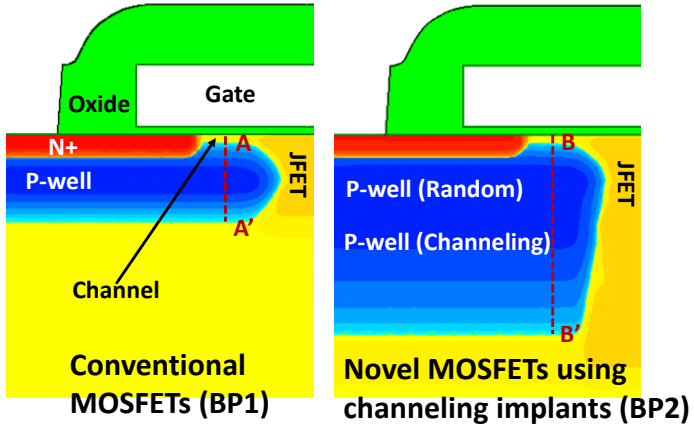
Technical Accomplishments and Progress



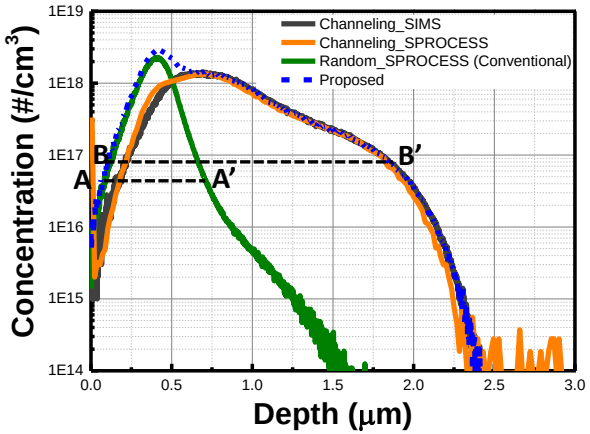
4 inch SiC wafer



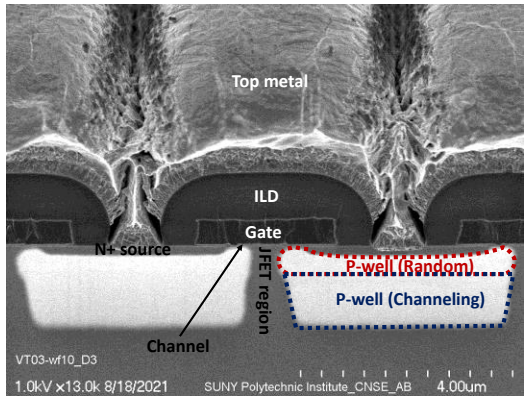
Packaged SiC MOSFETs



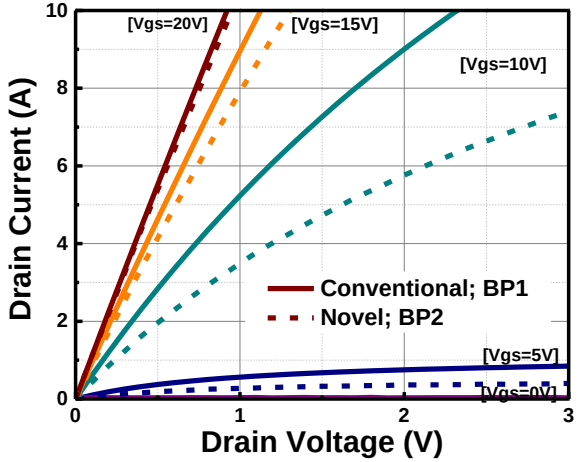
Cross-sectional view



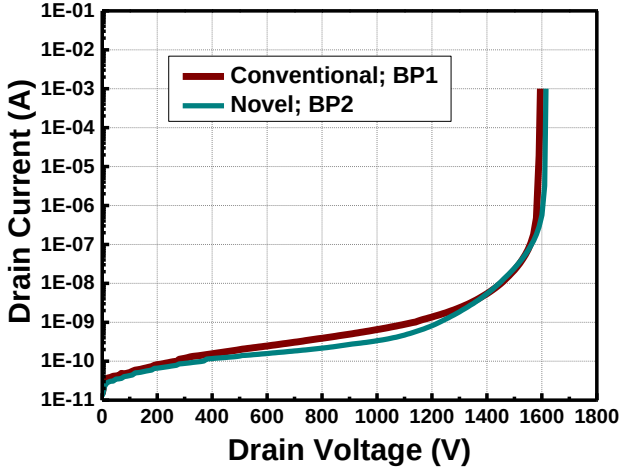
Implant profile



SEM image for novel MOSFETs

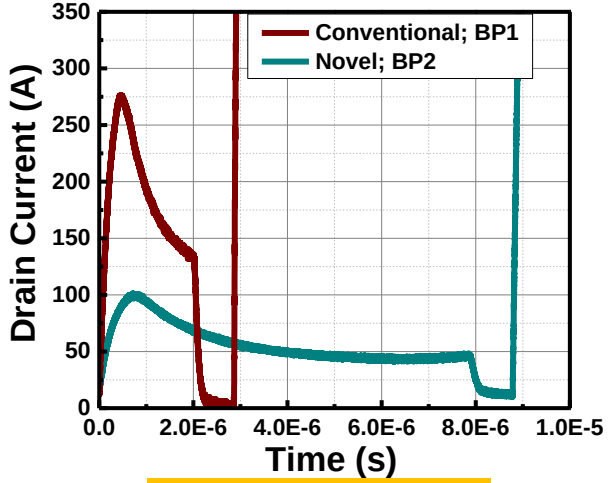


Output characteristics



Blocking behaviors

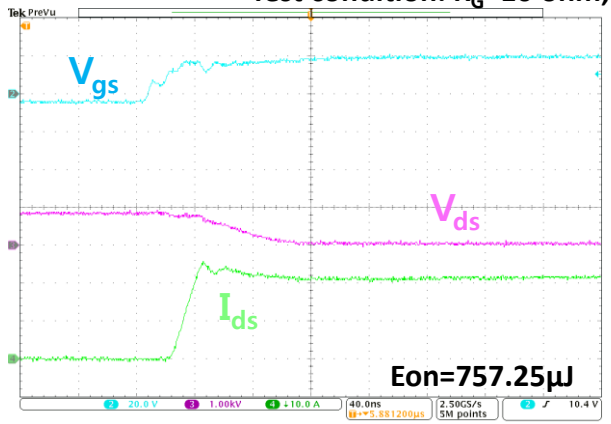
Test condition: R_G=20 ohm, V_{GS}=20V, V_{DS}=800V



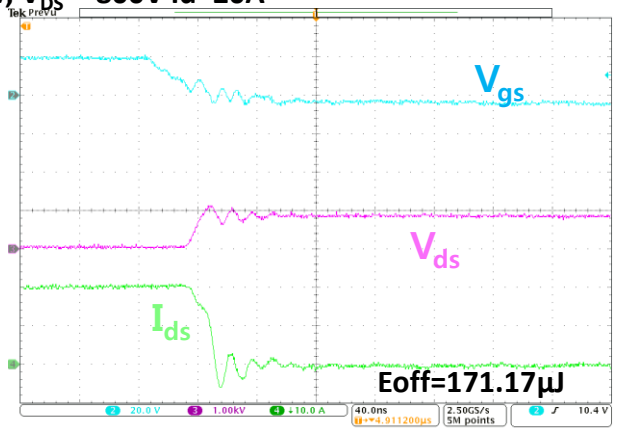
Short-circuit capability

Technical Accomplishments and Progress

Test condition: R_G=10 ohm, V_{GS}=20V/-4V, V_{DS}=~800V Id=20A

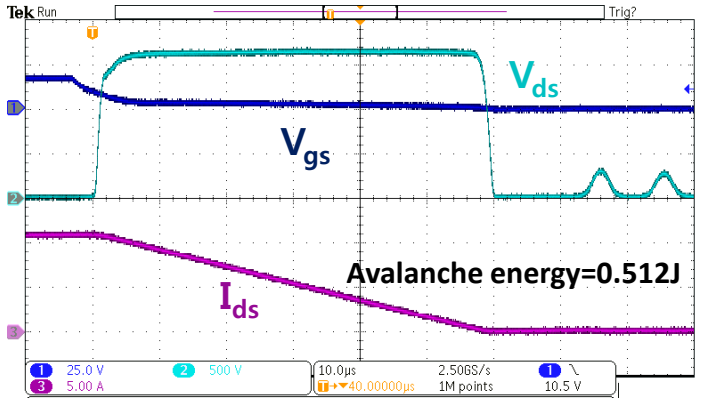


Switching Turn-on

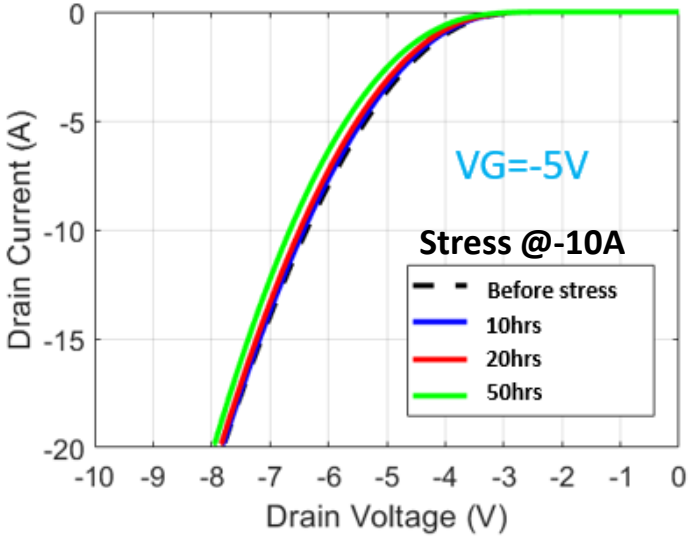


Switching Turn-off

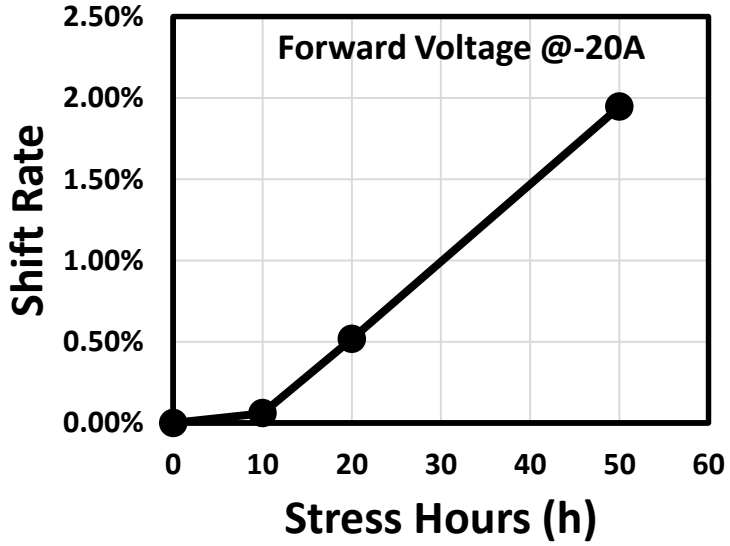
Test conditions: V_{DC}= 100V, L= 26mH



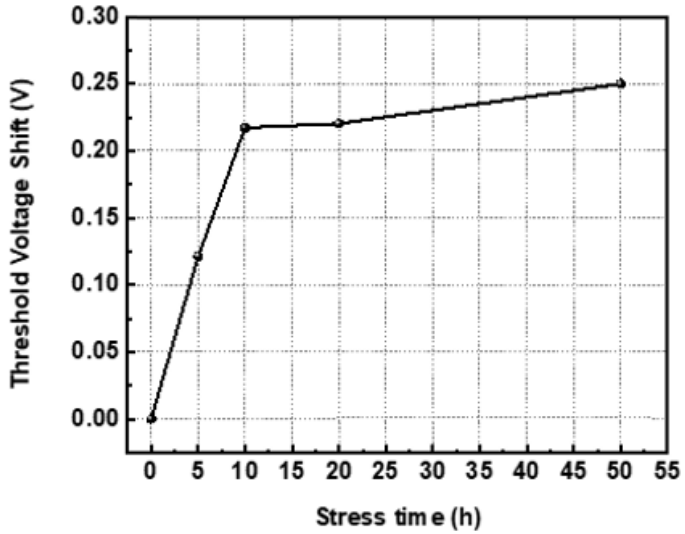
Avalanche energy



Body diode degradation



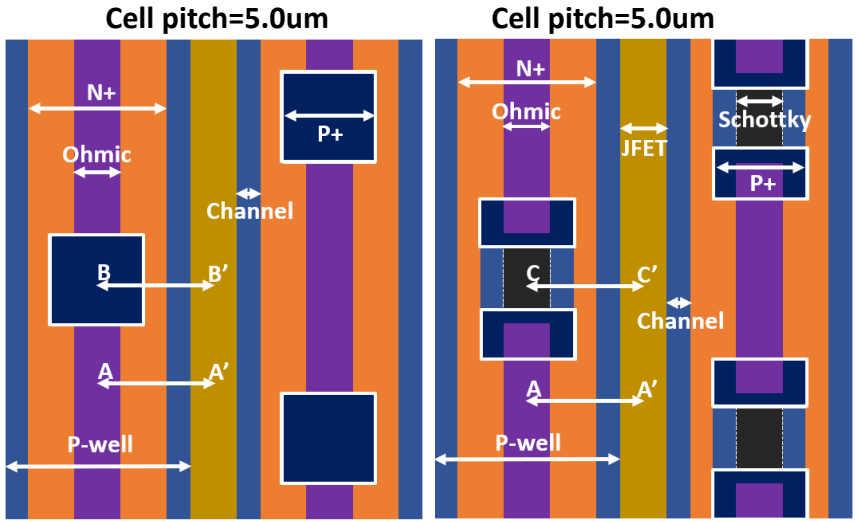
The change of V_F after body diode stress



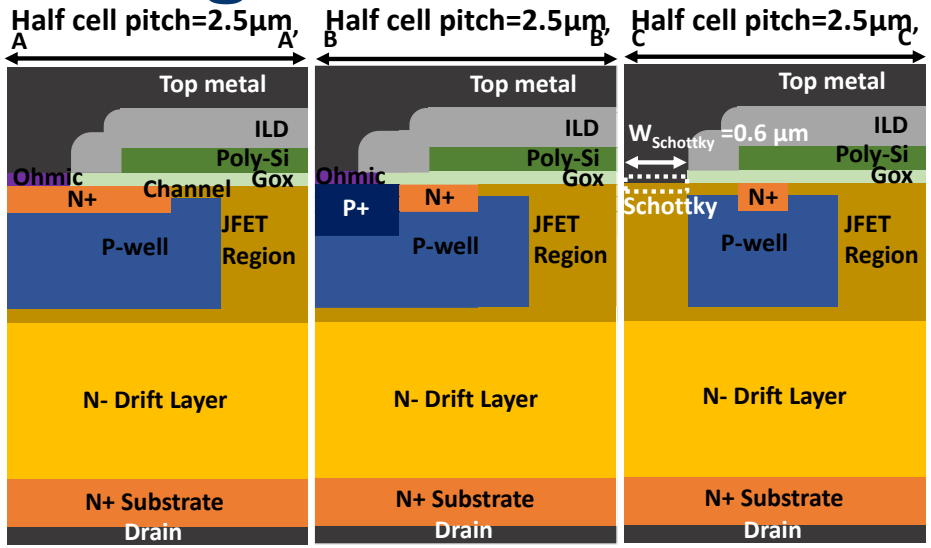
PBTI: Vgs=+20V

Switching, Avalanche, Body diode, and PBTI were measured at OSU

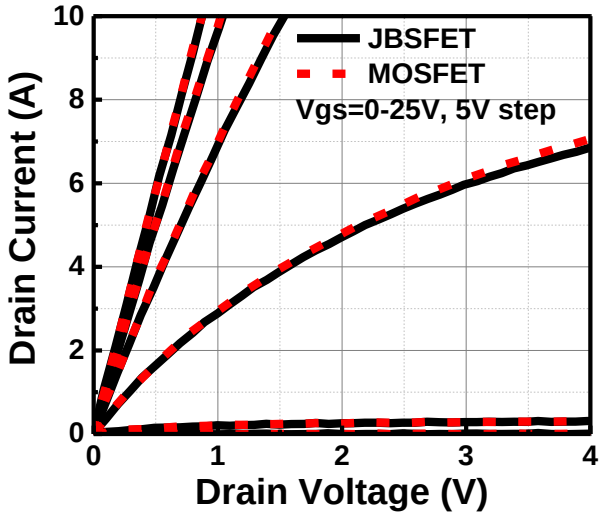
Technical Accomplishments and Progress



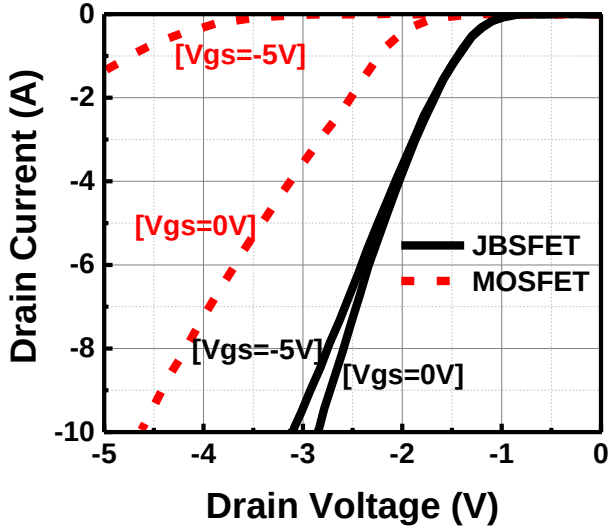
MOSFETs JBSFETs



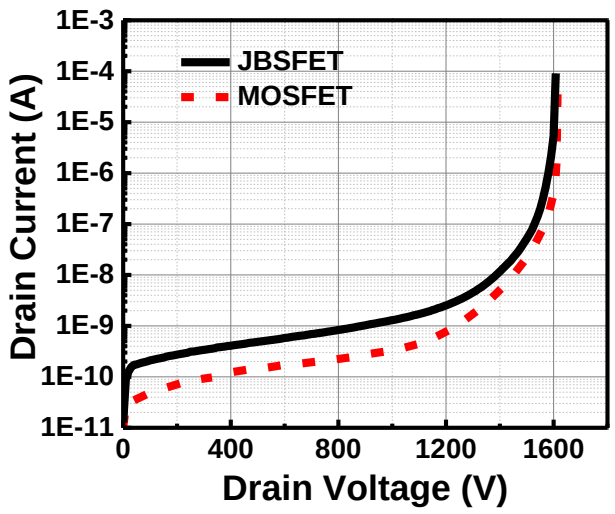
Cross-sectional view



Output characteristics



Third quadrant characteristics

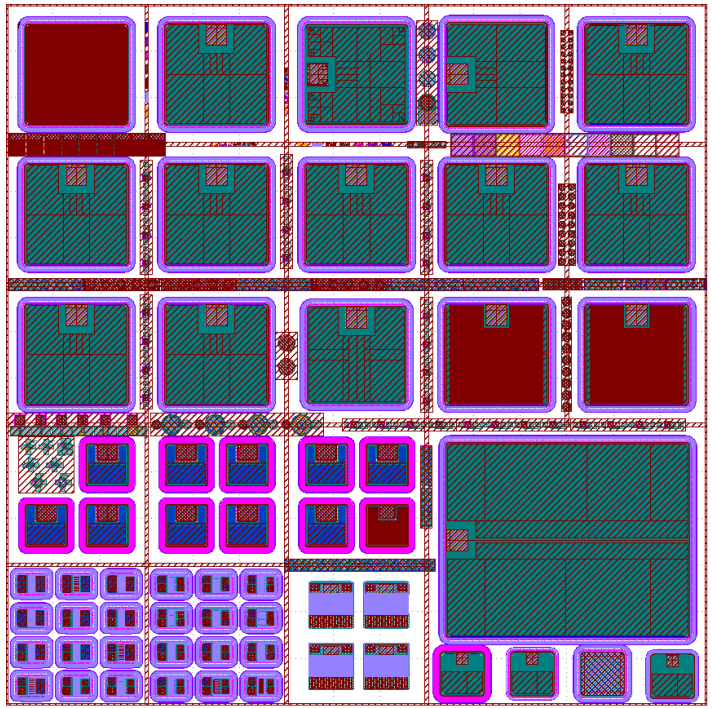


Blocking behaviors

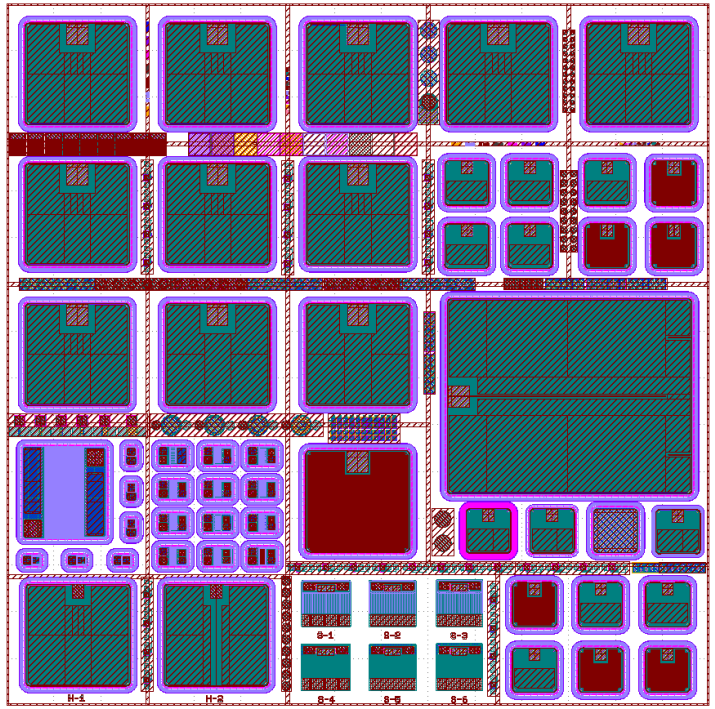
Technical Accomplishments and Progress

- **Mask design – floor plan for 1st and 2nd lot**

- PiN diode, JBS diode, MOSFETs (different sizes), JBSFETs and test structures were included.
- Mask design was taped out – design review by SiCamore engineers, kerf (process monitoring boxes) insertion was completed.



BP3-lot1



BP3-lot2

Collaboration and Coordination

	Collaboration	Relationship	Comments
SiCamore	Multiple projects	Fabrication service	SiCamore is providing process services for government projects that SUNY Poly leads.
The Ohio State University	Multiple government projects	Partner for EDTC project	OSU will evaluate reliability as well as performances of devices that SUNY fabricated.
Sandia National Laboratories	EDTC	Leading national lab	SNL and team members in EDTC will evaluate devices
ARL / ONR	MUSiC	Funding agency	Currently developing 12kV SiC MOSFETs
National Renewable Energy Laboratory	EDTC	Partner for EDTC project	NREL will package 1.2kV MOSFETs from SUNY Poly for double side cooling system

Remaining Challenges and Barriers

Fabrication resources

- Multiple resources in U.S. need to be secured.

Process readiness

- Critical processes such as gate oxide formation need to be developed for high channel mobility;
- SiCamore currently outsources some processing steps such as ion implantations (High energy);

Packaging research

- Advanced packaging research is one of important aspects in reducing the chip cost.

Proposed Future Research

Process development

- Gate oxide process for high mobility and high quality will be developed;
- Channeling implants and room temperature implants will be optimized;

Device innovation

- Cell structure and edge termination area will be optimized in terms of performance (static and dynamic) and reliability;

Reliability assessment

- Collaboration with OSU - Feedback on the design of device and process.

Packaging research

- High voltage, high temperature, high performance packaging will be developed.

Summary

	Device information	$R_{on,sp}$	BV	Body diode degradation	PBTI	Avalanche energy	SC SOA	Switching Turn-on/Turn-off
D1	Conventional P-well with Lch=0.5um	3.98 mΩ-cm^2	1667V	<Δ 2%	Δ+0.25V	In progress	In progress	In progress
D2	Deep P-well with Lch=0.5um	4.12 mΩ-cm^2	1615V	In progress	In progress	512mJ	~8us	0.757/ 0.171mJ
D3	Deep P-well with Lch=0.3um	3.35 mΩ-cm^2	1609V	In progress	In progress	In progress	~5us	0.449/ 0.180mJ

- Static characteristics, reliability, and ruggedness test were conducted on packaged devices from BP2.
- Two mask designs for fabrication were generated.
- The SC SOA was significantly improved using deep P-well structure.
- All aspects (CPR) need to be considered in a comprehensive research program.
- Strong team (fab and partner) was formed to accomplish the proposed goals.

Cost-Competitive, High-Performance, Highly Reliable Power Devices on Gallium Nitride

Principal Investigators: Shadi Sadvik

State University of New York Polytechnic Institute

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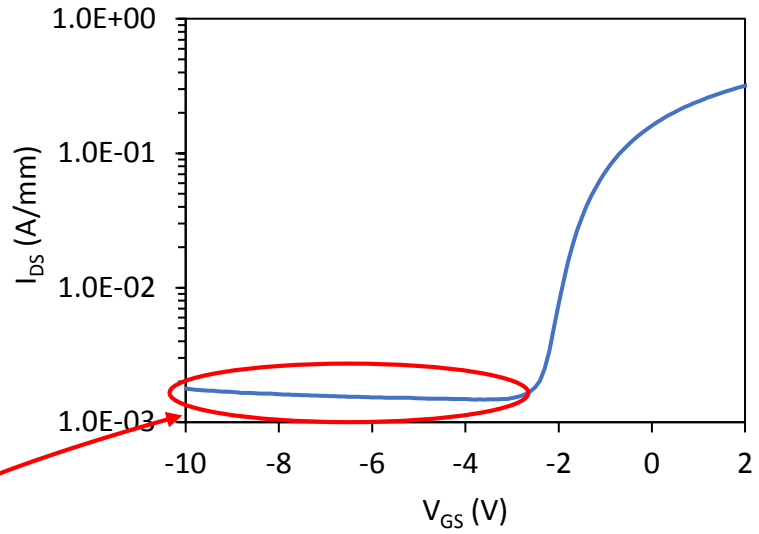
Project ID # elt247

Progress: Experimental Design to Reduce HEMT I_{OFF}



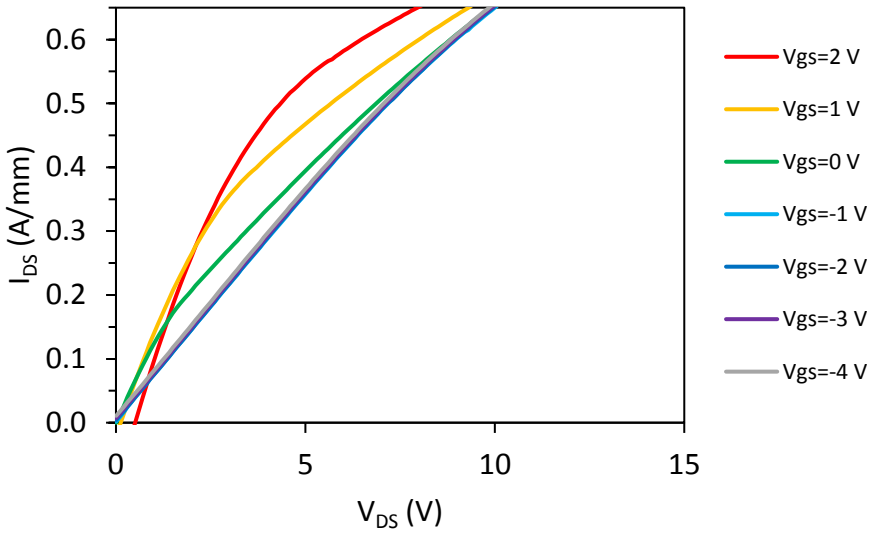
- With improved device isolation, good gate control observed in HEMTs
- I_{ON}/I_{OFF} still only ~10^2 due to high I_{OFF}
- High I_{OFF} believed to be due to bulk leakage in UID GaN channel layer
- Conduction in UID GaN due mostly to impurity incorporation (e.g., C and O)

- In order to decrease I_{OFF}, decreased background impurity concentrations in the UID GaN buffer/channel layer is desirable
- Our "normal" HEMT growth uses 100 Torr UID GaN layer to match 100 Torr AlGaN growth pressure
- Increasing GaN growth pressure to 300 Torr decreases [C], but additional ramp between GaN and AlGaN layers necessary

Four Growth Conditions:

- Constant 100 Torr growth pressure
- 300 Torr GaN followed by ramp to 100 Torr AlGaN
- 300 Torr GaN followed by ramp to 100 Torr with AlN interlayer before AlGaN
- 300 Torr GaN followed by ramp to 100 Torr GaN before AlGaN

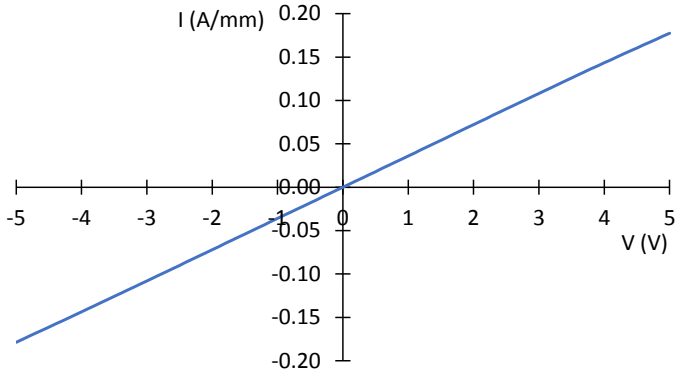
Challenge: High Leakage Likely due to Growth Issue



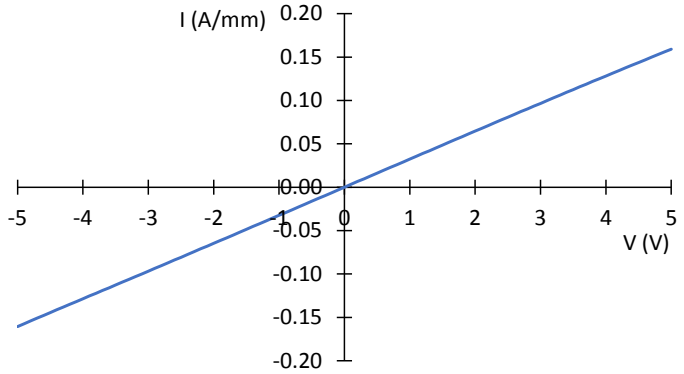
Output characteristics of HEMT with constant 100 Torr growth condition; this is the "normal" HEMT condition.

- Very high I_{OFF}, nearly no gate control observed in all devices, regardless of channel layer variation
- After initial devices showed poor characteristics, fabrication repeated using ion implant isolation instead of mesa etch
- Devices fabricated with modified process flow showed similar poor results

- High leakage between nominally isolated device areas measured, regardless of isolation technique
- Bulk leakage suspected; material optimization required
- GaN and AlGaN layers re-optimized



*I-V measurement between contacts of two different devices separated by **mesa etch**. Low resistance ohmic conduction indicates poor isolation.*



*I-V measurement between contacts of two different devices separated by **ion implant**. Low resistance ohmic conduction indicates poor isolation.*

Technical Progress Summary and Future Work

- Experiment designed to improve I_{ON}/I_{OFF} by modifying GaN channel layer in HEMT
- HEMTs fabricated and characterized
- All HEMTs have very poor gate control, bulk leakage believed to be cause
- Material growth optimized to improve electrical characteristics (decreased impurity/carrier concentration)

- While material optimization proceeds, AlGaN/GaN grown on both sapphire and bulk GaN purchased from outside vendor
- Fabrication is ongoing on purchased material alongside new material grown in-house
- Completion expected within 1-2 months